ERI Design: IDEA and POSH
MAGICAL: Machine Generated Analog IC Layout

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The University of Texas at Austin

IDEA and POSH Integration Open Session: Tutorial and Demo
Detroit, MI

July 17, 2019

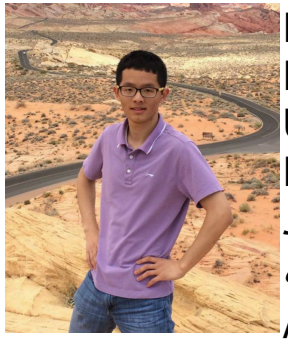
Program Overview

- Project "MAGICAL: Machine Generated Analog IC Layout" under IDEA TA-1
- MAGICAL subtasks/approaches
  - Task 1. Learning-based analog layout constraint generation
  - Task 2. Learning-based analog placement algorithm and software development
  - Task 3. Learning-based analog routing algorithm and software development
- Innovative claims
  - Leveraging human intelligence (e.g., designer experience, learning data)
  - Machine learning to help generate layout constraints (no human in the loop)
  - New placement and routing algorithms and software for quality of results and runtime (24-hour turn-around-time)
- MAGICAL input and output will be in industry standard formats
- Performer(s)
  - The University of Texas at Austin

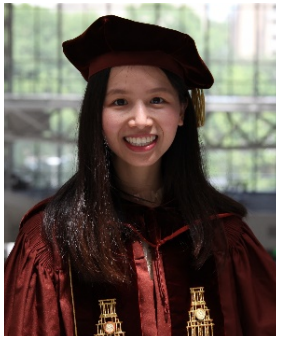
The MAGICAL Team

Prof. David Z. Pan (PI)
- PI, UT Faculty since 2003
- IBM Research 2000-2003
- UCLA PhD 2000
- Physical design, DFM, machine learning, FPGA, emerging technologies

Prof. Nan Sun (co-PI)
- Co-PI, UT Faculty since 2010
- Harvard PhD 2010
- Analog, mixed-signal IC design



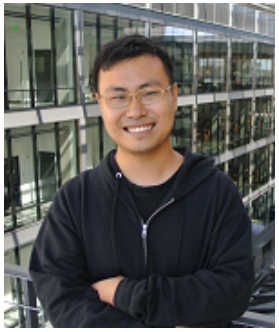
Dr. Yibo Lin
Postdoc, 2018-19
UT-ECE PhD 2018
PD, DFM, ML
Just joined PKU as an assistant professor



Dr. Biying Xu
BS, ZJU 2014;
PhD, UT Austin 2019;
Analog PD, ML
To join Cadence

Dr. Shaolan Li
Postdoc, 2018-19
UT-ECE PhD 2018
Analog/MS IC design
To join Georgia Tech as an assistant professor

Mingjie Liu
BS, PKU 2016;
MS, UMich 2018
Analog design, CAD, ML

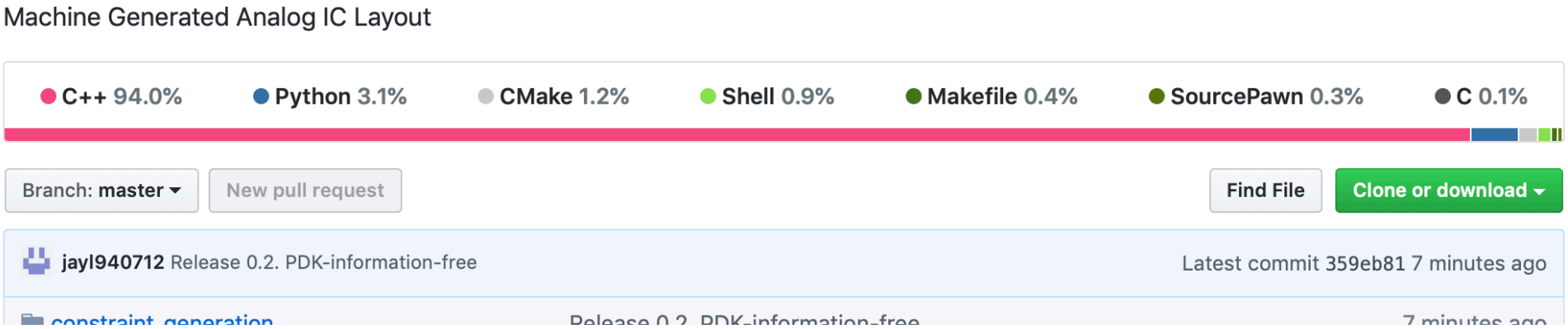


Keren Zhu
BS, UWisc 2016
MS, UT Austin 2018
Physical design

Xiyuan Tang
BS, SJTU 2012
MS, UT Austin 2014
Analog/MS IC design;
Graduate soon, will stay as a postdoc at UT

MAGICAL 0.2 Public Release

- Open-source code released in May 2019 (under BSD-3 license)
- GitHub: https://github.com/magical-eda/MAGICAL
  - **End-to-end** analog layout generation from netlist to GDSII
  - **No dependency** on commercial tools
  - **Push-button, no-human-in-the-loop**
  - **Include** toy techfiles and circuit examples for demonstration (PDK-related information removed); capable of handling real PDK too
  - Device generation released in binary due to NDA issue



MAGICAL: Circuit Benchmark Release

- Open-sourced sanitized benchmark circuits (PDK-stripped): https://github.com/magical-eda/MAGICAL-CIRCUITS
  - Python script to strip out PDK-related information
  - **26 circuits** from real taped-out quality designs, including ADC cores, comparators, OTAs, and buffers

Branch: **master** ▾ **MAGICAL-CIRCUITS** / **benchmark_circuits** /

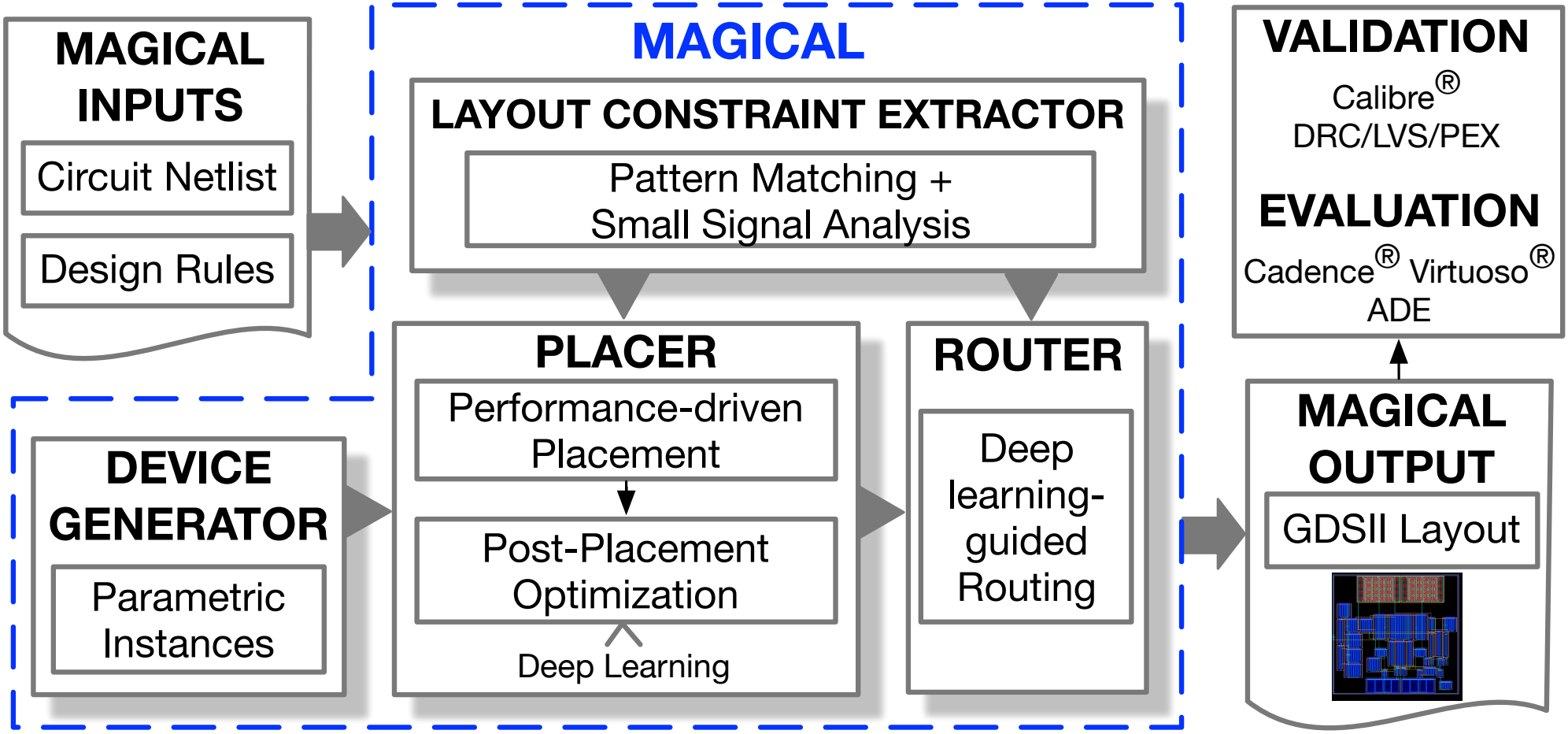
jayl940712 Update vrefp_buffer

..	
ADC	initial release of ADC, comparator and OTA circuits
Comparator	initial release of ADC, comparator and OTA circuits
OTA	initial release of ADC, comparator and OTA circuits
Vcm_Buffer	Update vrefp_buffer
Vrefp_buffer	Update vrefp_buffer

```
* label = OTA
.subckt Gm1_v5_Practice ibias vdd vim vip vom vop vss
xm8 net074 ntail1 vss vss hvtnfet w=w0 l=l0
xm2 vdd ibias vdd vdd lvtpfet w=w1 l=l1
xm4 vdd ibias vdd vdd lvtpfet w=w1 l=l1
xm12 ibias ibias vdd vdd lvtpfet w=w2 l=l0
xm11 vom ibias vdd vdd lvtpfet w=w3 l=l0
xm15 ibias ibias vdd vdd lvtpfet w=w2 l=l0
xm14 vop ibias vdd vdd lvtpfet w=w3 l=l0
xm26 vop vim net074 net074 lvtnfet w=w4 l=l0
xm27 vom vip net074 net074 lvtnfet w=w4 l=l0
xc21 ntail1 vom vss cap
xc22 vop ntail1 vss cap
xr12 ntail1 vop vss res
xr11 vom ntail1 vss res
xm3 vss ntail1 vss vss lvtnfet w=w5 l=l2
xm0 vss ntail1 vss vss lvtnfet w=w5 l=l2
d0 net074 vdd diode
d1 vss vdd diode
.ends Gm1_v5_Practice
```

PDK-Stripped netlist of an OTA

MAGICAL Overview



Subtask 1: Layout Constraint Generation

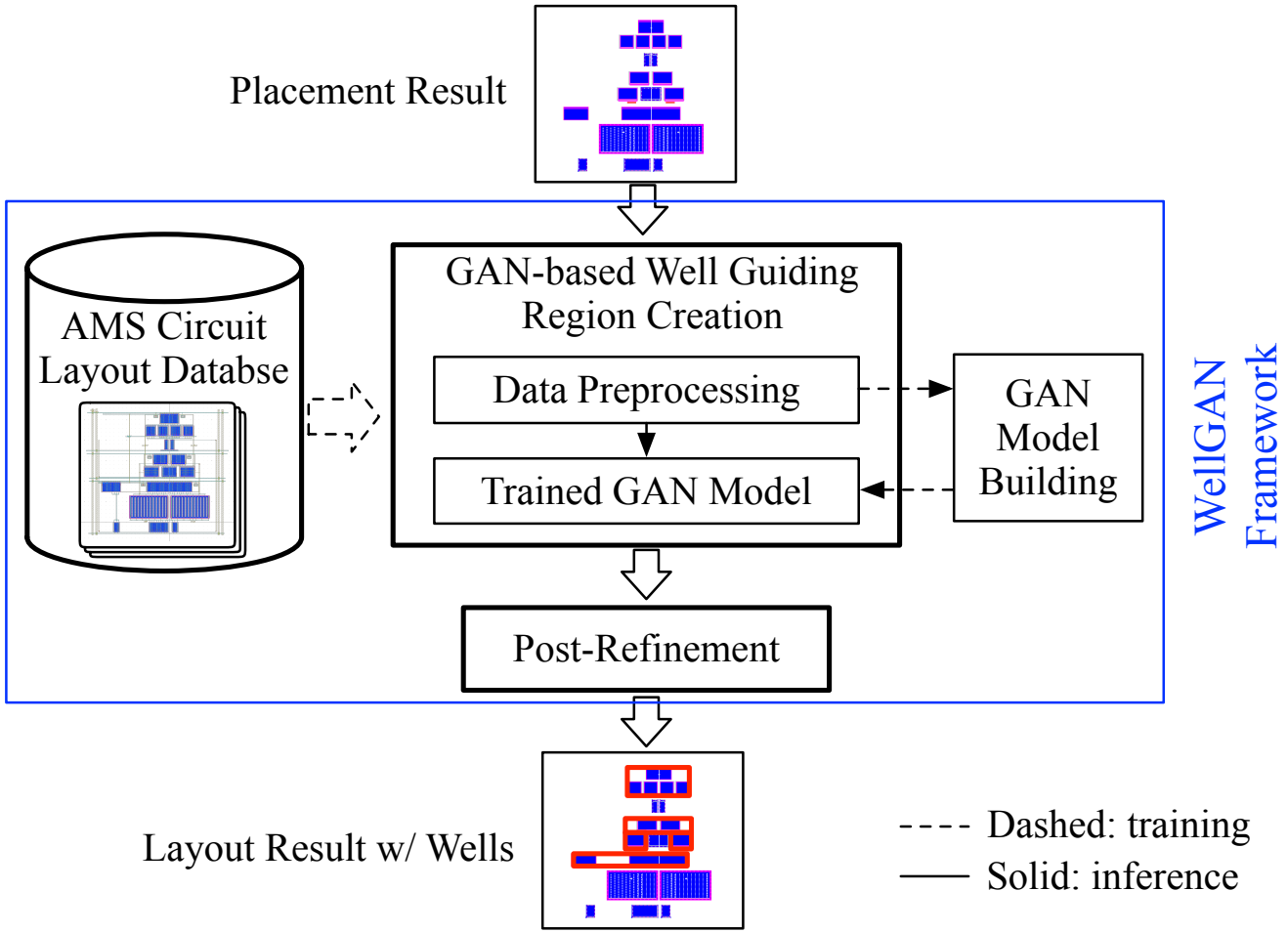
- MAGICAL 0.1 (Jan. 2019 integration version):
  - Used pattern matching and signal flow analysis
  - Effective for device constraints in small circuit blocks, e.g., comparator, operational amplifier, OTA
- MAGICAL 0.2 Release:
  - Improved symmetry constraint robustness
- More under research and development:
  - Working towards hierarchical design and constraint extraction
  - Implemented different approaches to predict **system level** symmetry constraints using various graph-based techniques
  - Implemented critical net prediction based on graph learning

Subtask 2: Analog Placement

- MAGICAL 0.1:
  - Device generation leveraging Virtuoso PCell generation tool
  - Analytical analog placement that support symmetry constraints
  - GAN-based well generation for polygonal well island shapes
- MAGICAL 0.2 Update:
  - Remove third party commercial software dependency in both device generation and placement stage;
  - Support both symmetry constraints and net criticality/weighting
  - Improve placement **robustness** (e.g., increase spacing between devices for better routability)
  - More robust well generation supporting different options: polygonal, rectangular, and individual wells if applicable
- More under research and development:
  - **Performance driven** placement with machine learning

WellGAN – Deep Learning Guided Well Generation

- Well generation using generative adversarial networks to learn experienced designers' layout behavior [Xu+, DAC'19]
- Achieve well generation results similar to manual designs

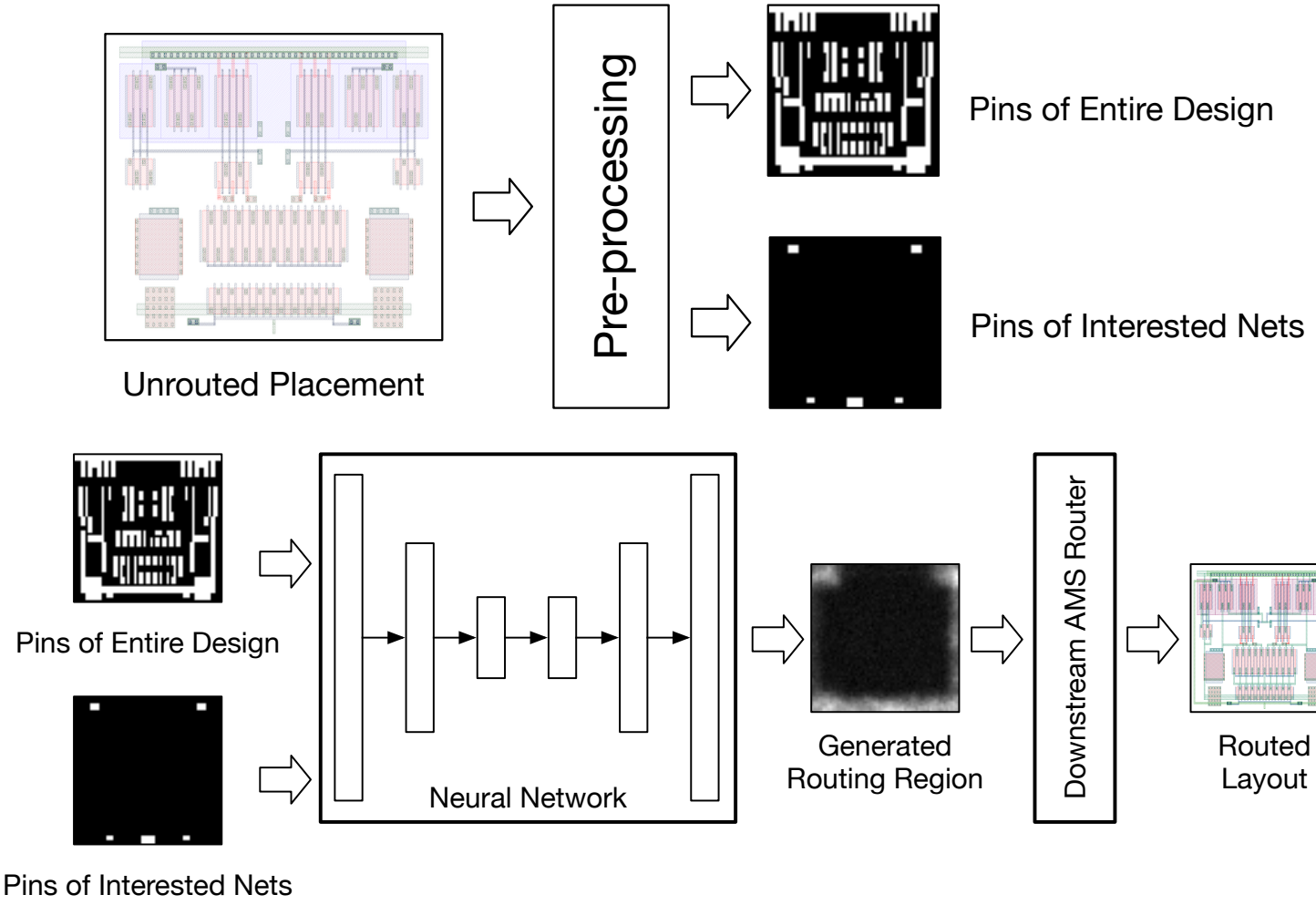


Subtask 3: Analog Routing

- MAGICAL 0.1:
  - A* search-based routing
  - Negotiation-based rip-up and reroute
  - Handle symmetric net pairs and self-symmetric nets
- MAGICAL 0.2 Update:
  - Improve efficiency by integrating global routing in the flow
  - Improve router robustness
- New results:
  - Machine learning-based analog routing - GeniusRoute [Zhu+, ICCAD'19]
- More under research and development:
  - **Performance driven** routing with machine learning

GeniusRoute Framework [Zhu+, ICCAD'19]

- Learn different routing strategies for specific types of nets from manual layouts using deep neural networks
- Apply learned knowledge to guide automatic routing



GeniusRoute Results [Zhu+, ICCAD'19]

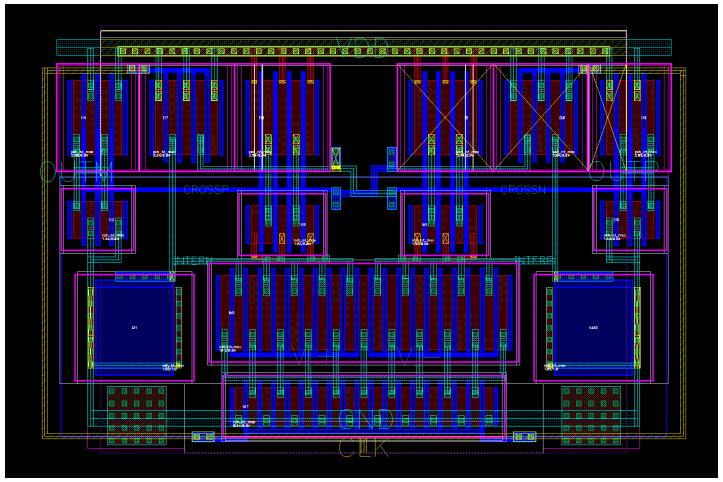
Comparator	Schematic	Manual	Magical 0.1 Router	GeniusRoute
Offset (uV)	/	480	2530	830
Delay (ps)	102	170	164	163
Noise (uVrms)	439.8	406.6	438.7	420.7
Power (uW)	13.45	16.98	16.82	16.80

OTA	Schematic	Manual	Magical 0.1 Router	GeniusRoute
Gain (dB)	38.20	37.47	36.61	37.36
PM (degree)	64.66	72.46	94.68	76.40
Noise (uVrms)	222.0	223.7	292.7	224.8
Offset (mV)	/	0.88	3.21	0.39
CMRR (dB)	/	59.61	58.52	59.15
BW (MHz)	110.5	102.5	232.1	107.3
Power (uW)	776.93	757.35	715.11	787.82

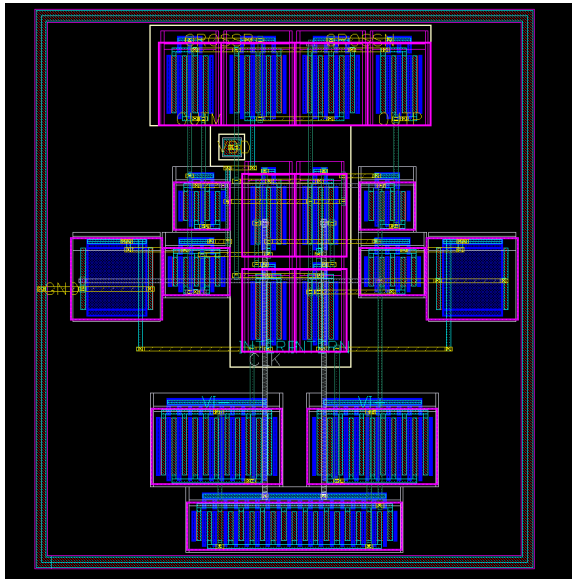
MAGICAL 0.2 Results (I)

Post-Layout Simulation Results of a Comparator (TSMC 40nm)

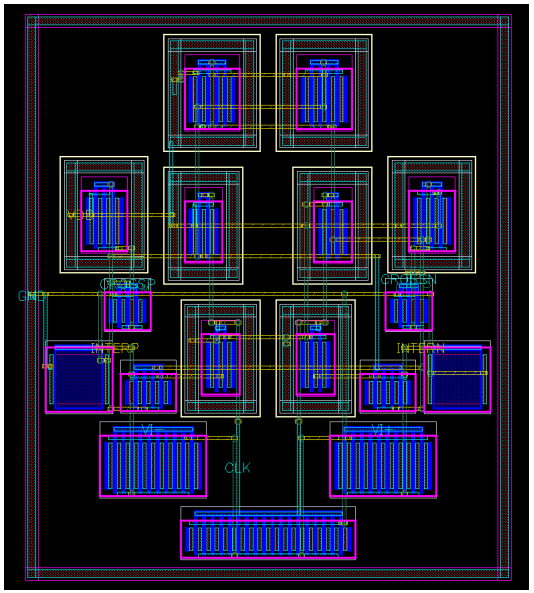
Metric	Manual	MAGICAL 0.1	MAGICAL 0.2
Output Delay (ps)	150	185	152
Input-referred Noise (uVrms)	380	367	334
Input-referred Offset (mV)	0.151	1.43	0.5



Manual Layout



MAGICAL 0.1 Layout

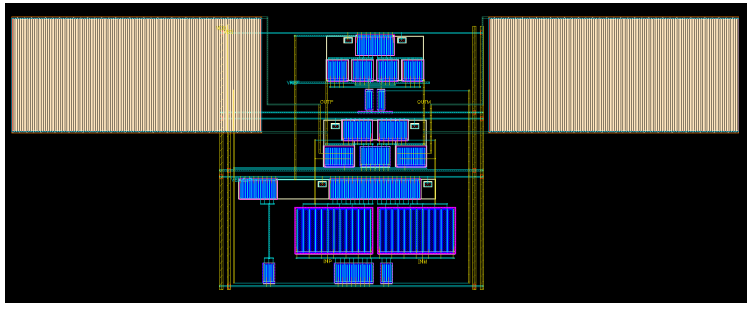


MAGICAL 0.2 Layout

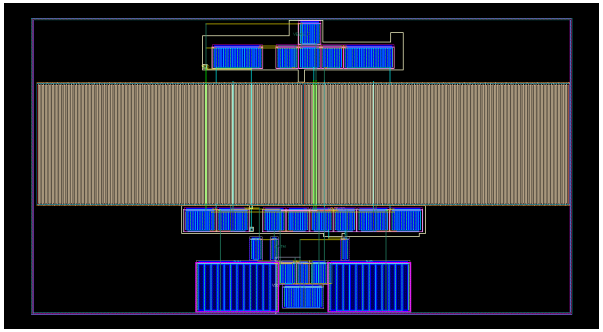
MAGICAL 0.2 Results (II)

Post-Layout Simulation of a Miller Compensation OTA (TSMC 40nm)

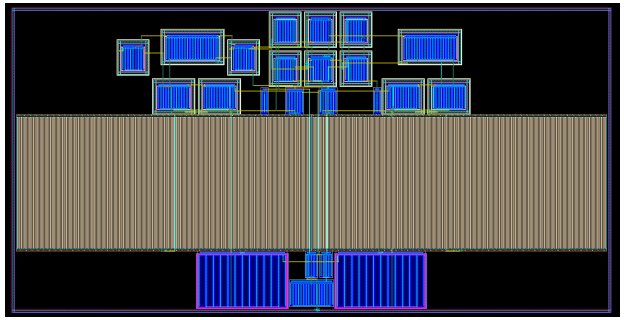
Metric	Manual	MAGICAL 0.1	MAGICAL 0.2
DC Gain (dB)	37.7	37.5	38
Unity-gain Bandwidth (MHz)	110	105	107.5
Phase Margin (degree)	67.8	65	62.3
Input-referred Noise (uVrms)	219	223	221.5
CMRR (dB)	103	89	92.5
Input-referred Offset (mV)	0.2	2	0.48



Manual Layout



MAGICAL 0.1 Layout

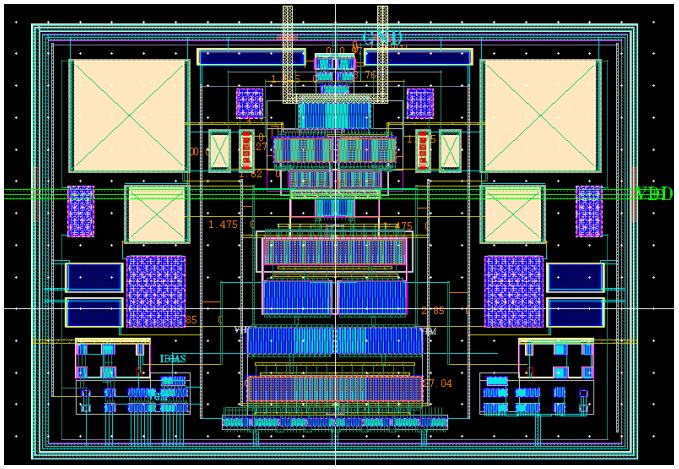


MAGICAL 0.2 Layout

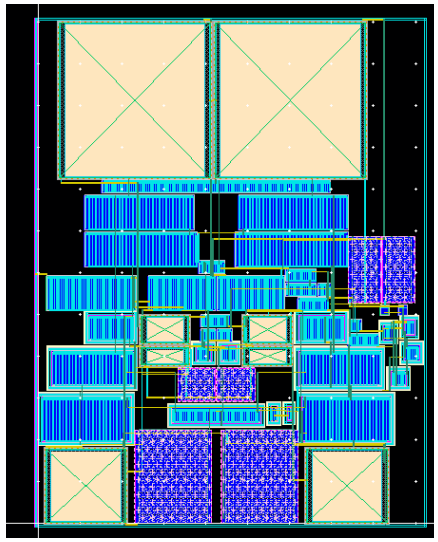
MAGICAL 0.2 Results (III)

Post-Layout Simulation of an Inverter-Based Feed-Forward OTA (TSMC 40nm)

Metric	Manual	MAGICAL 0.2
DC Gain (dB)	69	69
Unity-gain Bandwidth (MHz)	1300	1130
Phase Margin (degree)	58	56.5
CMRR (dB)	94.5	110
Input-referred Offset (mV)	0.016	0.001



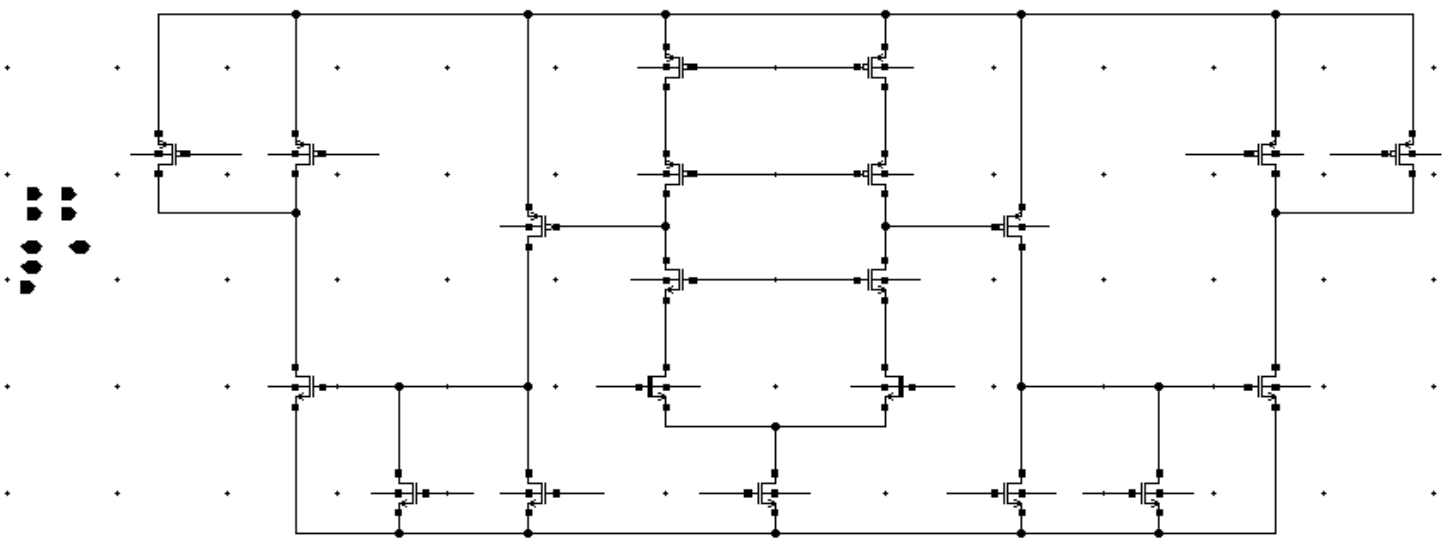
Manual Layout



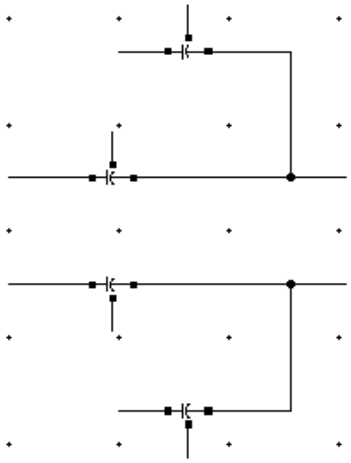
MAGICAL 0.2 Layout

MAGICAL 0.2 Demo of a More Complicated Circuit

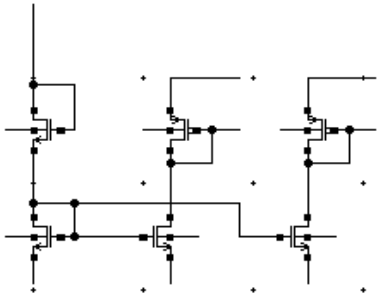
3-stage Nested-Miller OTA



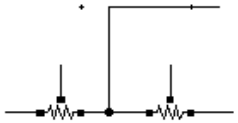
Gain Stage



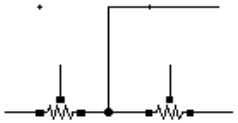
Miller Capacitors



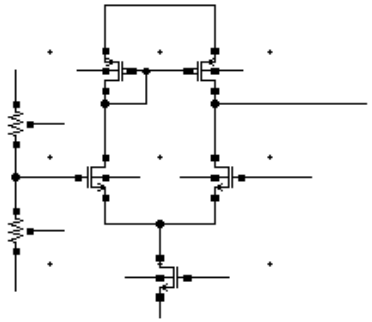
Bias



CMFB1

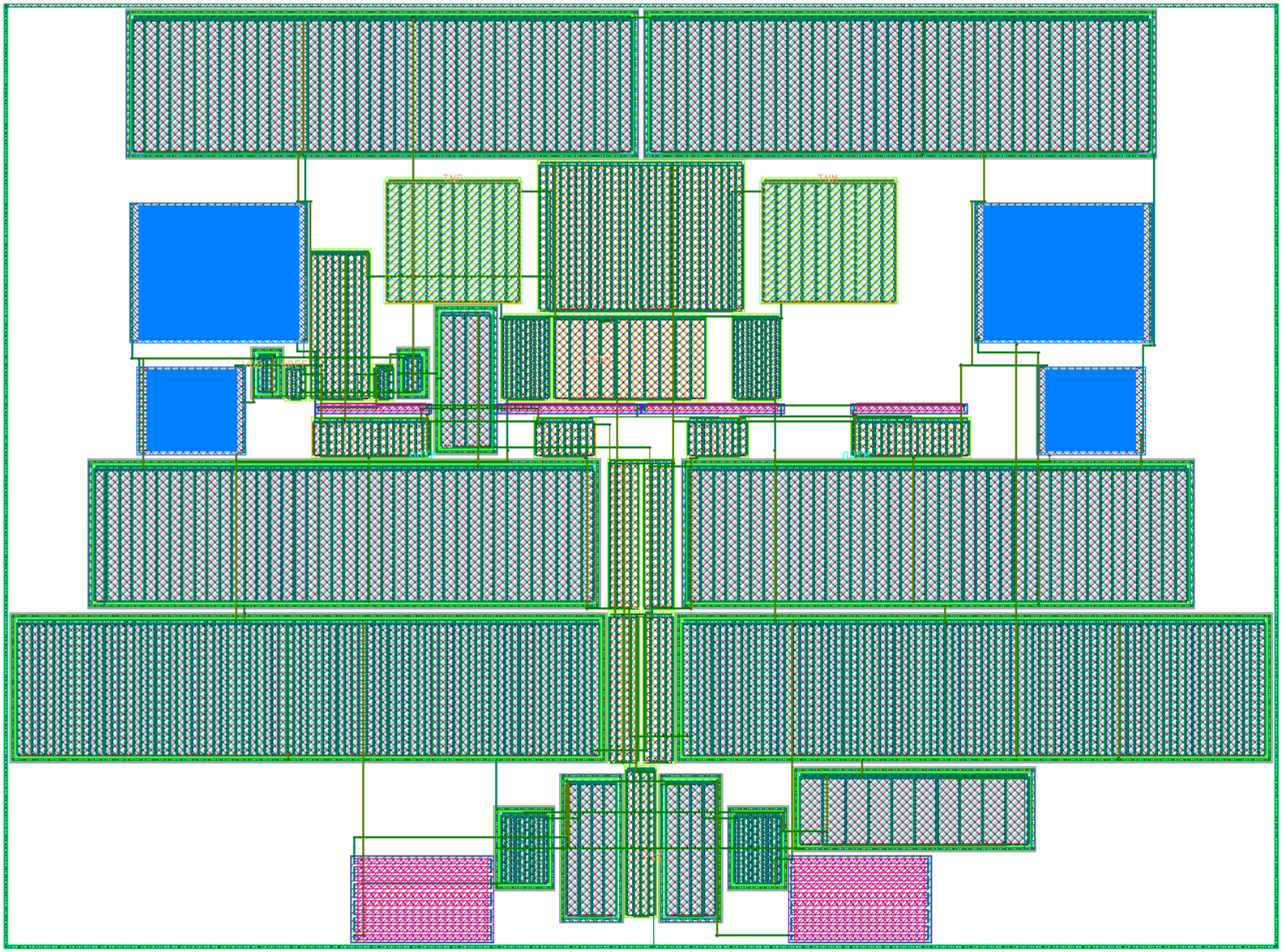


CMFB2



CMFB3

MAGICAL 0.2 Layout of 3-stage Nested-Miller OTA

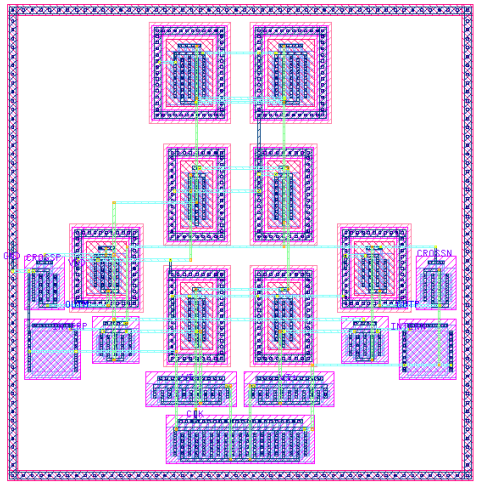


MAGICAL 0.2 Simulation Results

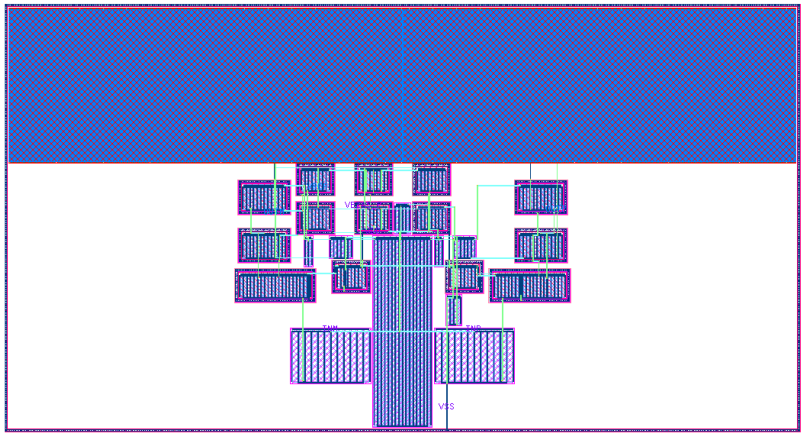
Post-Layout Simulation of the 3-stage Nested-Miller OTA

Metric	Schematic	MAGICAL 0.2
DC Gain (dB)	59.81	62.51
Unity-gain Bandwidth (MHz)	29.54	26.72
Phase Margin (degree)	72.11	65.6
CMRR (dB)	/	95.53
Input-referred Offset (uV)	/	0.2

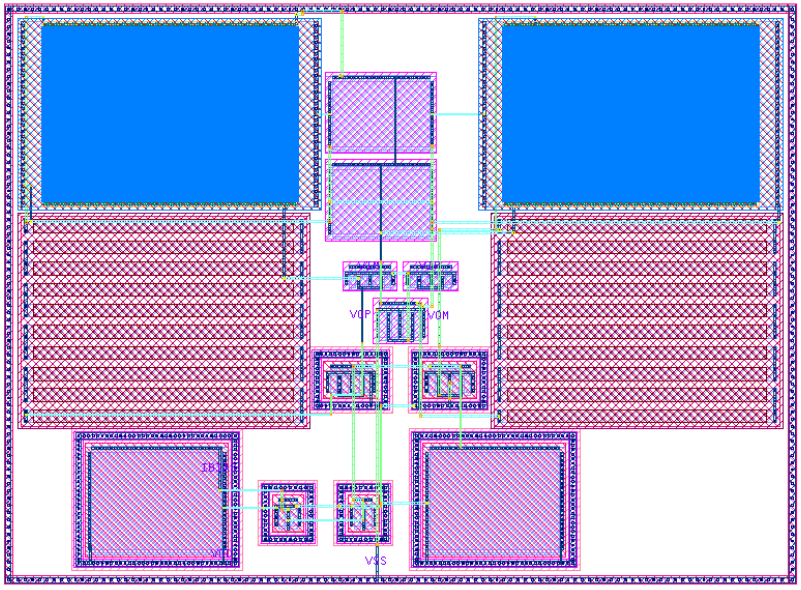
MAGICAL 0.2 Layouts of More Circuits



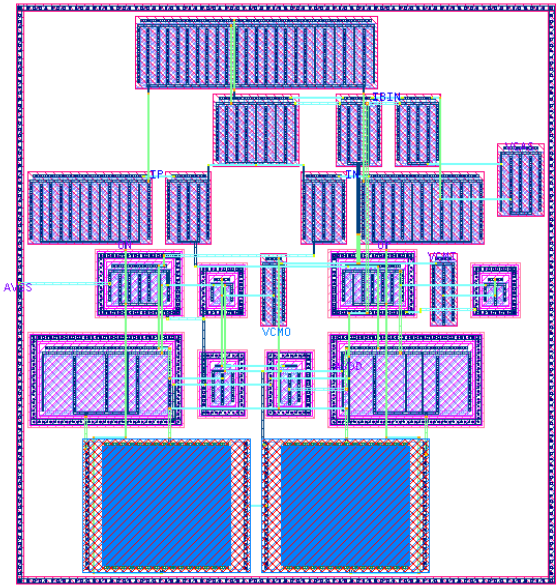
Comparator



OTA_1



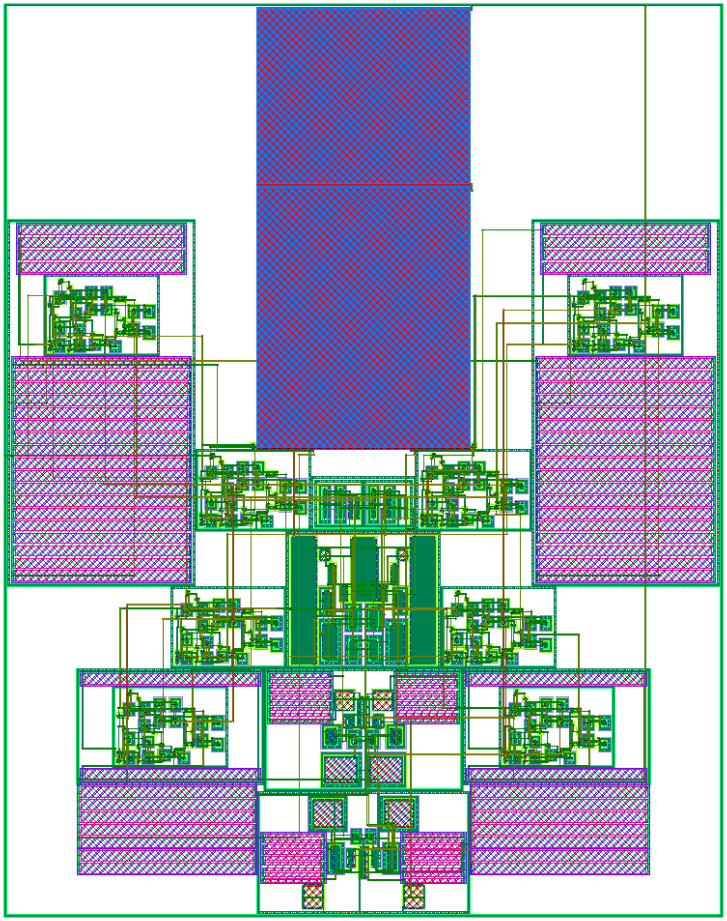
OTA_2



OTA_3

MAGICAL Hierarchical Flow: Preliminary Results

- MAGICAL hierarchical flow under development
  - Combination of Python for easy extensibility and C++ for high efficiency
- Preliminary result of CT-DSM (continuous-time ΔΣ modulator)



with manual constraints at this time; still integrating with system-level constraint generation

MAGICAL Publications

- Biying Xu, Shaolan Li, Chak-Wa Pui, Derong Liu, Linxiao Shen, Yibo Lin, Nan Sun, and David Z. Pan, "Device Layer-Aware Analytical Placement for Analog Circuits," *ACM International Symposium on Physical Design (ISPD),* San Francisco, CA, April 14-17, 2019. (Best Paper Award Nomination)
- Biying Xu, Yibo Lin, Xiyuan Tang, Shaolan Li, Linxiao Shen, Nan Sun, and David Z. Pan, "WellGAN: Generative-Adversarial-Network-Guided Well Generation for Analog/Mixed-Signal Circuit Layout, " *ACM/IEEE Design Automation Conference (DAC),* June 2-6, 2019.
- Keren Zhu, Mingjie Liu, Yibo Lin, Biying Xu, Shaolan Li, Xiyuan Tang, Nan Sun, and David Z. Pan, "GeniusRoute: A New Analog Routing Paradigm Using Generative Neural Network Guidance," *IEEE/ACM International Conference on Computer Aided Design (ICCAD),* Nov. 4-7, 2019.

https://github.com/magical-eda/MAGICAL

Q & A